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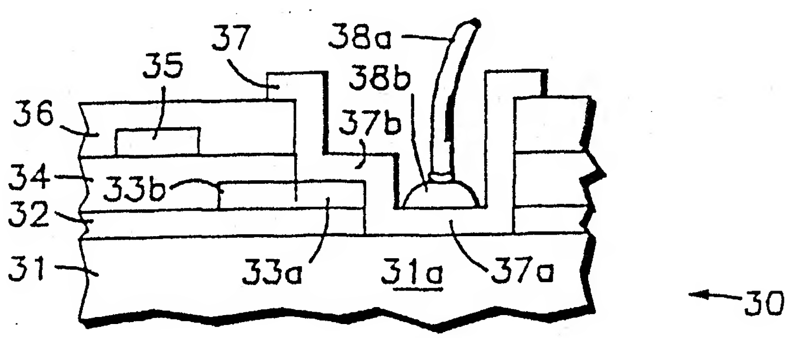
(54) Title: IMPROVED BONDING MEANS AND METHODS FOR POLYMER COATED DEVICES



FOURTH MASK

(57) Abstract

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IMPROVED BONDING MEANS AND METHODS FOR POLYMER COATED DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates, in general, to means and methods for forming bonding regions on electrical devices, and more particularly, to improved structures and manufacturing processes for forming bonding pad regions on electrical devices containing comparatively soft dielectric layers, such as polymers, and to improved electrical devices utilizing these improved structures and processes.

Background Art

Electrical devices such as transistors, integrated circuits, bubble memories, sensors, and Josephson devices make extensive use of dielectric layers for a wide variety of functions, for example, as insulating layers, as structural or chemical buffer layers, as mechanical support layers, as planarizing layers, as passivation layers, and/or as masking layers. Frequently, a dielectric film may be required to play several roles at the same time. When that is the case, materials well suited for one use may be less than ideal for another, and a different combination of materials or a different structure is generally required. This can create problems of increased fabrication complexity.

An example of this situation occurs in the design of bubble memories where polymer layers, such as polyimides, are used as a buffer layer between the magnetic substrate and the metallic circuit elements which generate and guide the magnetic domains in the substrate. If the metal conductors are deposited directly on the substrate, large differential stresses can be generated which adversely

relieves this stress and performance is improved. Refractory oxides and/or nitrides can provide some stress relief, but polymer or other organic films have been found to be most effective for this purpose. The organic films provide another advantage of great utility in that they also act as planarizing layers, that is, they help to smooth out surface irregularities which are frequently present. Organic dielectrics are particularly suitable as stress relief and planarizing layers because they are comparatively soft and flexible. Unfortunately, these same characteristics make them poor surfaces for supporting the metal bonding pads which must be provided for attachment of external lead wires. Thus, in device structures (e.g. bubble memories, integrated circuits, sensors, discrete devices, Josepheson devices, and the like) where organic polymer layers are used to support metallic bonding pads, there is reduced bonding yield and bond strength. This increases costs and reduces reliability.

Accordingly, it is desirable that the bonding pads rest on a portion of the device which is not supported by the comparatively soft organic layer. Where multiple conductor layers are utilized, separated by dielectric interlayers, the problem of providing a comparatively rigid support for the bonding pads becomes more complex. In the prior art, firmly supported bonding pads have been achieved by adding additional process steps so that the portions of the metal conductors to be used for bonding are formed directly on the harder substrate, while the other portions can be formed on the softer organic layers. Adding process steps reduces the manufacturing yield and increases the cost of fabrication, above what would otherwise be required. Thus, a need continues to exist for improved means and methods for providing improved, firmly supported, bonding pads on electrical devices in which comparatively soft organic dielectric layers are otherwise used by

Accordingly it is an object of the present invention to provide an improved electrical device having at least one conductor layer resting on an organic dielectric layer, and adapted to use multiple conductor layers separated by one or more interlayer dielectrics, and wherein one or more bonding pad regions are situated on and firmly supported by the substrate so as to provide improved bonding characteristics, and wherein the bonding pad regions are electrically connected to at least one conductor layer.

It is an additional object of the present invention to provide the above described improved device, wherein the bonding pad regions and the electrical connections between the bonding pad regions and the at least one conductor layer lie external to the organic stress relief layer and the optional interlayer dielectric.

It is a further object of the present invention to provide the above described improved device utilizing a polymer, optionally a polyimide, as the organic dielectric and, optionally, utilizing a substrate having an insulating region underlying the bonding region.

It is an additional object of the present invention to provide an improved process for fabricating the above described electrical device structure without adding additional process steps.

SUMMARY OF THE INVENTION

In a first embodiment of the invention, an improved electrical device is provided comprising a substrate and at least one conductor layer overlying and substantially separated from the substrate by a first dielectric layer softer than the substrate, at least one additional dielectric layer overlying and covering a portion of the conductor layer, and a metallic conductor adapted for bonding; wherein the metallic conductor adapted for bonding

conductor layers and extends to and rests on the substrate to provide a bonding pad region supported directly by the substrate, and wherein the metallic conductor adapted for bonding is substantially external to both the first dielectric layer and any additional dielectric layer or layers which lie between conductor layers. A substrate having a refractory insulating region underlying the bonding region is optionally utilized.

In a second embodiment of the invention, the improved electronic device described above is provided wherein the first dielectric is an organic layer, preferably a polymer, further, wherein the additional dielectric layers are also polymers, preferably but not only a polyimide.

In a third embodiment of the invention, an improved process for fabricating an electrical device structure on a substrate is provided, comprising: forming a dielectric layer on the substrate; forming a first conductor on a portion of the first dielectric layer, the first conductor having a contact region and a device region; forming a second dielectric layer on at least a portion of the first conductor; removing the second dielectric layer from the contact region to substantially expose the contact region; removing the first and second dielectric layers from a portion of the substrate to expose the portion of the substrate; applying a metallic conductor which contacts and interconnects the exposed portion of the substrate and the contact region; and providing on the exposed portion of the substrate and directly supported thereby, a portion of the metallic conductor adapted to bonding.

In a fourth embodiment of the invention, the above described improved process is provided, further comprising, prior to the removing steps, preparing a second conductor on a portion of the second dielectric layer, wherein the second conductor includes a contact portion, and the metallic conductor contacts the contact portion of the

first conductor, and wherein the contact portion of the second conductor overhangs the first conductor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified cross-section of a portion of an electronic device structure, according to the prior art, utilizing an organic stress relief layer between the substrate and a first conductor layer, and having a bonding pad region connected to the first conductor layer, and supported by the organic stress relief layer.

FIGS. 2A-E are simplified cross-sections of a portion of a prior art device during various stages of manufacture, and with an alternate conductor arrangement so that the bonding pad region is supported by the substrate.

FIGS. 3A-D are simplified cross-sections of a portion of a device structure of the present invention during various stages of manufacture.

FIGS. 4A-E are simplified cross-sections of a portion of a device structure of the present invention during various stages of manufacture, and according to a further embodiment.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 shows portion 10 of an electronic device structure of the prior art, comprising substrate 11, dielectric stress relief or isolation layer 12, first conductor layer 13, dielectric interlayer 14, second conductor layer 15, and passivation layer or protective coating 16. Conductor 13 has portion 13a on which a bonding pad is to be formed, and portion 13b which comprises or connects to an active region responsible for device action. No particular active regions are shown in device portion 10. Conductor 17 is formed with bonding pad

3. Bonding wire 18a is attached to bonding pad portion 17a by bond 18b. Bonding pad portion 17a overlies portion 13a of conductor 13, which rests on portion 12a of stress relief layer 12 covering portion 11a of substrate 11. The structure of FIG. 1 has the drawback that bonding pad portion 17a is supported by stress relief layer 12 in region 12a. Thus, when a comparatively soft organic material is used for layer 12, poor bonding stength and bonding yield result. It will be recognized by those of skill in the art that conductors 13, 15, and 17 can be of the same or different materials, provided that layer 17 is suitable for bonding.

FIG. 2E, also formed according to the prior art, shows electronic device portion 20 comprising substrate 21, comparativity soft stress relief or isolation layer 22, first conductor layer 23, interlayer dielectric 24, second conductor layer 25, passivation or protective layer 26, and bonding layer 27. First conductor layer 23 has contact portion 23a which makes contact to bonding layer 27 in region 27a, and active portion 23b which comprises or connects to active regions of device portion 20. No particular active regions are shown in device portion 20. Bonding pad portion 27a of bonding layer 27 rests on contact portion 23a of first conductor layer 23 which rests in turn on portion 21a of substrate 21. Bonding wire 28a is attached to bonding layer 27 by bond 28b on bonding pad portion 27a. The device configuration of FIG. 2E permits bonding pad portion 27a to be supported by more rigid substrate 21 through first conductor layer 23. Thus, to the extent that conductor layer 23 of FIG. 2E is harder or less resilient than organic isolation layer 12 of FIG. 1, as is usually the case, then the bonding characteristics of the structure of FIG. 2E are improved relative to the structure of FIG. 1. However, as will be readily apparent to those of skill in the art

structure of FIG. 1. Thus the manufacturing cost is undesirably increased.

The masking sequence to arrive at the structure of FIG. 2E is shown schematically in FIGS. 2A-E. In FIG. 2A, substrate 21 is coated with dielectric stress relief or isolation layer 22, and portion 22a of layer 22 is removed by methods well known in the art utilizing a first mask pattern. First conductor layer 23 is then applied and etched using a second mask pattern to give conductor 23a-b shown in FIG. 2B. Methods for applying and patterning conductor layers are well known in the art.

Dielectric interlayer 24 is then applied (FIG. 2C) over layer 22 and conductor 23a-b, and second conductor layer 25 is applied and patterned using a third mask. Layer 24 and conductor 25 are covered by passivation or protective layer 26. In FIG. 2D, a fourth mask is used to open access hole 29 in layers 24 and 26, exposing contact portion 23a of layer 23. Bonding layer 27 is then applied and patterned (FIG. 2E) using a fifth mask to give bonding pad portion 27a covering contact portion 23a of layer 23. Methods for forming layers 22-27 and patterning layers 22-27 are well known in the art. Bonding wire 28a is attached by bond 28b to bonding pad portion 27a of bonding layer 27. Thermo-compression or ultrasonic bonding may be used. Five masking layers are required to form this prior art structure.

The method of formation and structure of a first embodiment of the present invention is shown in FIGS. 3A-D. In FIG. 3A, substrate 31 has formed thereon stress relief and/or dielectric isolation layer 32. Substrate 31 may be a conductor, a semiconductor, an insulator or a combination thereof depending on the desired device function. First conductor layer 33 is applied and patterned into conductor 33a-b using a first mask layer. Conductor layer 33 has contact portion 33a, and active portion 33b which comprises

particular active regions are shown in device portion 30 of FIGS. 3A-D. The active regions are not important to the present invention. The composition of the material of first conductor layer 33 will depend upon the device function desired to be performed, and is readily chosen by one of skill in the art once the device function is defined.

In FIG. 3B, interlayer dielectric 34 is applied without masking to cover first conductor 33a-b. A second conductor layer is formed thereon and patterned, using a second mask, to give conductor 35. Passivation or protective layer 36 is optionally applied. In FIG. 3C, opening 39 is formed, using a third mask, to expose both contact portion 33a of first conductor layer 33 and support portion 31a of substrate 31. It is convenient that portions 31a and 33a be adjacent to reduce the number of large steps, i.e. regions of different height, that must be covered by layer 37 between portions 33a and 31a. Bonding layer 37 is then applied and patterned in FIG. 3D using a fourth mask. Bonding layer 37 has bonding pad portion 37a which is directly supported by portion 31a of substrate 31, and contact portion 37b which is electrically connected to contact portion 33a of conductor layer 33. Bonding wire 38a is connected to bonding pad portion 37a of bonding layer 37 by bond 38b. Four masking steps are required to fabricate the structure of FIG. 3D. It will be readily apparent that bonding layer 37 lies external to layer 32 and layer 34 and rests directly on substrate 31.

The present invention provides the desired result of locating the bonding pad directly on the comparatively rigid substrate, and in one less manufacturing step. Other things being equal, the manufacturing cost to fabricate the device structure of FIG. 3D will be reduced by the ratio 4/5 as compared to the prior art device of FIG. 2E. The device structure of FIG. 3D [illegible]

without the latter's deficiency of having the bonding pad region supported by the comparatively soft dielectric stress relief layer. Hence, the method and structure of the present invention, illustrated in FIGS. 3A-D, is particularly advantageous when dielectric layer 32 and/or interlayer dielectric layer 34 are formed from a comparatively soft organic material.

The process described above is applied to the construction of magnetic bubble memory devices of improved characteristics. Substrate 31 is a magnetic garnet, and stress relief layer 32 is formed from a polyimide. Type PI-2555 polyimide supplied by E.I. DuPont, Inc., Wilmington, Delaware, is found to give satisfactory results. Polyimide layer 32 is formed by diluting the polyimide in N-Methyl-2-Pyrrolidone solvent in the ratio 80-25% solvent to 20-75% polyimide by volume, and placing a drop of the mixture on the surface of the substrate which is then spun at high speed. Excess material is automatically thrown off the edge. Layer thicknesses in the range 0.03 to 1.0 μm are obtained with 0.1 μm being convenient. The layers are typically baked at 350°C for 120 minutes in an inert ambient. Other polymers and solvents are also useful. Techniques for applying such layers are well known in the art. Conductors 35 and 33a-b are formed, for example, from an alloy of Ni-Fe and a sandwich structure of Cr/Cu/Cr respectively. Bonding layer 37 is formed typically from a sandwich structure of Cr/Au, with the Au outermost to provide a surface adapted for bonding. Interlayer dielectric 34 and protective layer 36 are also formed from polyimide, following substantially the same procedure as described for layer 32. Methods for forming dielectric layers 32, 34, and 36, and conductor layers 33, 35, and 37 are well known in the art. Conductor layers 33 and 35 may be formed from metals, semiconductors, semi-metals, or a combination thereof. Bonding layer 37 must be of a material suitable for bonding, typically a

metal. Aluminum and gold are common examples of materials known to be suitable for bonding, but others are also useful.

Bubble memories made using the above materials, and the method and structure of FIGS. 3A-D, were equivalent to comparable structures built as in FIG. 1, in terms of the improved memory performance resulting from the use of an organic stress relief layer, i.e. layer 12 of FIG. 1 and layer 32 of FIG. 3D, but gave improved bonding yield and bond reliability relative to the prior art stucture of FIG. 1. Bubble memories made according to the method and structure of FIGS. 3A-D gave equivalent performance to those having the structure of FIG. 2D using the same materials, but gave higher yield and lower manufacuring cost, due to the elimination of the additional masking step required in the prior art process of FIGS. 2A-E.

FIGS. 4A-E show an alternative embodiment of the present invention in which bonding layer 47 contacts second conductor layer 45, and in which substrate 41 includes a semiconductor device or a portion of an integrated circuit. In FIG. 4A, device portion 40 has substrate 41 including emitter region 41a, base region 41b, collector region 41c, and optional isolation diffusion region 41d. Regions 41a-d have been previously prepared by methods well known in the art. Substrate 41 is covered with refractory dielectric layer 41g and organic layer 42, typically a polyimide. Openings 51-52 are provided in layers 41g and 42 to permit contact to emitter contact region 41e and base contact region 41f. Methods for applying and patterning layers 41g and 42 are well known in the art.

In FIG. 4B, first conductor layer 43 is applied on layer 42 and patterned into conductor portions 43a-b, to contact, respectively, base contact region 41f and emitter contact region 41e. First conductor portions 43a-b are covered (FIG. 3C) by interlayer dielectric 44 and second

into connected portions 45a-b. Passivation or protective layer 46 covers interlayer dielectric 44 and second conductor layer portions 45a-b. Methods for forming layers 44-46 and patterning layer 45 are well known in the art. An organic polymer, such as a polyimide can be conveniently, but not exclusively used for layers 44 and/or 46.

In FIG. 4D opening 49 is cut through layers 46 and 44 using an additional masking step. Contact portion 45a of second conductor layer 45 is exposed. Portion 41h of refractory dielectric layer 41g, resting on portion 41d of substrate 41 is also exposed. Methods for forming opening 49 are well known in the art. Bonding layer 47 is then applied (FIG. 4E) and patterned to form bonding pad portion 47a and contact portion 47b. Bonding pad portion 47a rests on portion 41h of refractory dielectric layer 41g. Contact portion 47b is electrically connected to second conductor layer portion 45a. Bonding wire 48a is attached to bonding pad portion 47a by bond 48b. Refractory dielectric 41g is provided to permit bonding pad portion 47a to be rigidly supported by, but electrically insulated from semiconductor substrate portion 41d. Where bonding pad portion 47a is desired to make electrical contact to semiconductor substrate portion 41d, portion 41h or all of layer 41g can be omitted. Bonding layer 47 need not be entirely external to passivation layer 46, but must be external to layers 42 and 44. For the purposes of this invention, refractory dielectric layer 41g can be considered as being an integral part of substrate 41. Contact portion 45a of second conductor layer 45 must extend beyond, i.e. overhang, first conductor layer portions 43a-b where it is desired that bonding layer 47 contact only second layer 45, that is, not short portions 45a and 43b together. The present invention is not restricted to the particular semiconductor device structures shown.

It will be apparent to those of skill in the art that the method and structures described above provide an improved electronic device configuration wherein organic layers may be used, underlying one or more conductor layers, without interfering with the ability to provide bonding layers having bonding pad regions directly supported by the substrate or a comparatively hard refractory dielectric or other material layer lying on the substrate, and further that the invented structure can be fabricated by the same number of process steps required for structures in which the bonding pads rest directly on a comparatively softer organic layer, and in fewer process steps than the prior art structures which place the bonding regions directly on the substrate. It will also be apparent to those of skill in the art that the improved structures permit improved device performance by virtue of the use of polymer layers therein, particularly polyimides, without suffering a degradation in bonding properties and bond reliability. It will be further apparent that the improved process and structure reduce the manufacturing costs relative to the prior art process and structures, by virtue of improved yield and fewer process steps compared to the prior art, for the same or improved device performance.

Those of skill in the art will also recognize that variations can be made on the process and structure of this invention without departing from the spirit and scope thereof. In particular, although the invention has been illustrated for substrates suitable for bubble memories or semiconductor devices and circuits, many different substrates can be used and similar results obtained provided that the substrates are comparatively harder than the organic layer or layers used in the device structure. It will be readily apparent, that metals, semiconductors, dielectrics, combinations thereof, and/or other

surface of the substrate adjacent to and/or underlying the bonding pad region without altering the essential elements of this invention. As used herein, the word "substrate" is intended to include such variations and complex structures. It will also be readily apparent that many different types of devices can use the process and structure of the present invention to obtain improved electrical and/or bonding performance at lower cost, for example, discrete devices, integrated circuits, sensors, Josephson devices, thin film resistors and capacitors, opto-electronic devices, acoustic devices, and the like. Further, it will be readily apparent that the present invention is useful wherever the substrate surface which is to support the bonding pad region is harder and/or less resilient than at least one of the superposed dielectric layers on which conductors are placed, irrespective of the material composition. Accordingly, it is intended to encompass all such variations.

Claims

1. In an electrical device having a substrate and at least one conductor layer overlying and separated from said substrate by a first dielectric, and a second dielectric overlying and covering a portion of said at least one conductor layer, wherein said first and second dielectrics are polymers, the improvement characterized by:

a metallic conductor adapted for bonding, in contact with a portion of said at least one conductor layer and extending to and resting on said substrate, to provide a bonding region resting directly on said substrate, and wherein said metallic conductor is substantially external to said both said first and second dielectrics.

2. In an electronic device structure having a substrate, an organic layer on said substrate, a first conductor on a first portion of said organic layer, a dielectric interlayer on said first conductor, a second conductor on said dielectric interlayer, said second conductor not overlying a contact portion of said first conductor, the improvement characterized by:

a third conductor adapted for bonding, formed in contact with said contact portion of said first conductor, lying external to said organic layer and said dielectric interlayer, and extending to said substrate to provide a bonding pad on said substrate.

3. An electric device structure on a substrate, comprising:

a first dielectric layer on a first portion of said substrate;

a first conductor on a portion of said first dielectric layer;

a second dielectric layer [illegible]

a second conductor on at least a portion of said second dielectric layer, and having a first portion suitable for contact;

a third conductor, adapted for bonding, contacting said first portion of said second conductor, and extending to said substrate to provide a bonding pad on said substrate.

4. The device structure of claim 3 wherein said third conductor lies external to all said dielectric layers.

5. The device structure of claim 4 wherein said first portion of said second conductor extends laterally beyond said first conductor so as to be in overhanging relation to said first conductor.

6. A process for fabricating an electrical device structure on a substrate, characterized by:

forming a first dielectric layer on said substrate;

forming a first conductor on a portion of said first dielectric layer, said first conductor having a contact region and a device region;

forming a second dielectric layer on at least a portion of said first conductor;

removing said second dielectric layer from said contact region of said first conductor;

removing said first and second dielectric layers from a portion of said substrate to expose said portion of said substrate;

applying a bonding conductor which contacts and interconnects said exposed portion of said substrate and said contact region of said first conductor and lies external to said first and second dielectric layers;

providing on said exposed portion of said substrate and directly supported thereby, a portion of said bonding

7. The process of claim 6 further comprising, prior to said removing steps, preparing a second conductor on a portion of said second dielectric layer, said second conductor not overlying said contact region of said first conductor.

8. A process for fabricating an electrical device structure on a substrate, characterized by:

forming a first dielectric layer on said substrate:

forming a first conductor on a portion of said first dielectric layer;

forming a second dielectric layer on at least a portion of said first conductor;

forming a second conductor on a portion of said second dielectric layer, said second conductor having ~~a~~ contact portion and a non-contact portion;

forming a third dielectric layer on said non-contact portion of said second conductor;

forming a third conductor, adapted for bonding, connected to said contact portion of said second conductor layer and extending to said substrate to provide thereon a bonding pad directly supported by said substrate.

9. The process of claim 8 further comprising locating said third conductor external to said first, second, and third dielectric layers, and overhanging said contact portion of said second conductor beyond an edge of said first conductor.

10. The process of claim 6 or 8 wherein at least one of said dielectric layers comprises a polyimide.

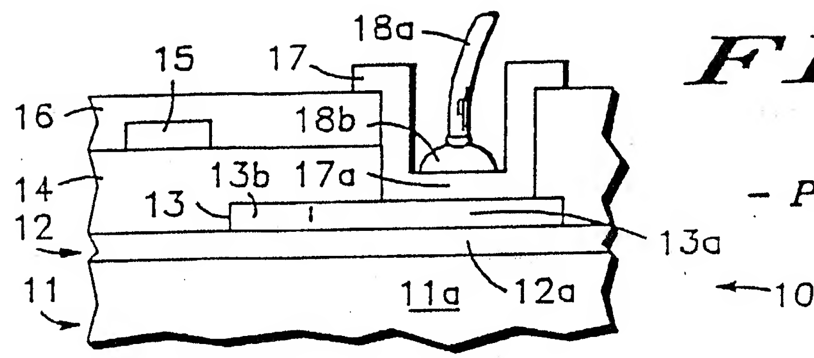

FIG. 1

- PRIOR ART -

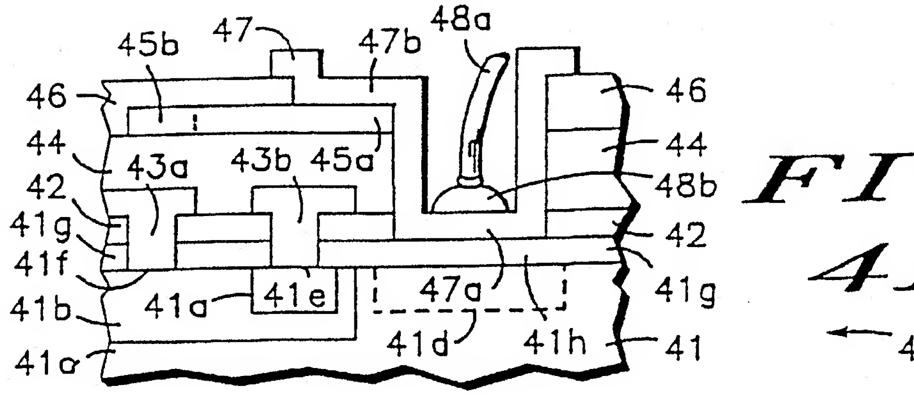

FIG. 4E

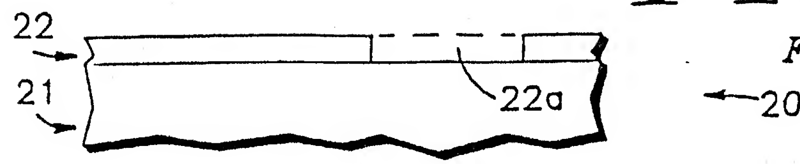

FIG. 2A

FIRST MASK

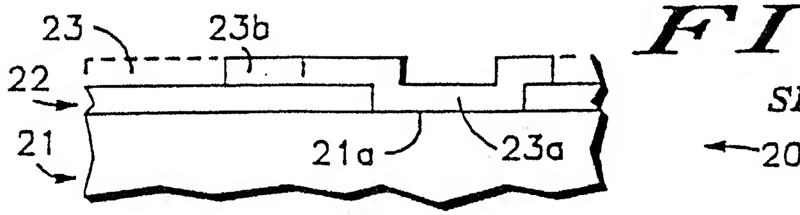

FIG. 2B

SECOND MASK

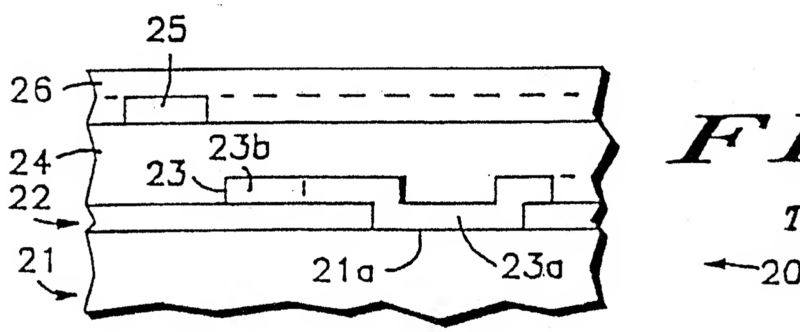

FIG. 2C

THIRD MASK

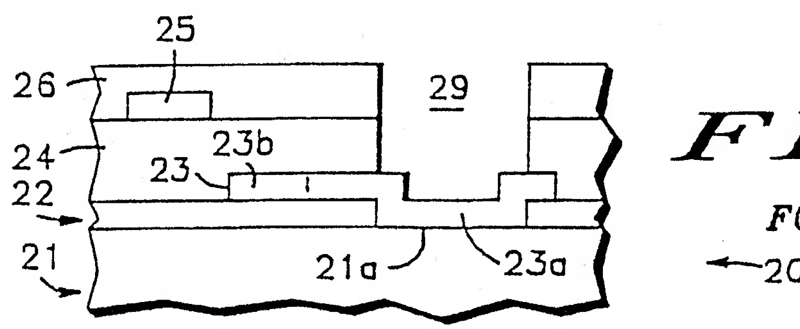

FIG. 2D

FOURTH MASK

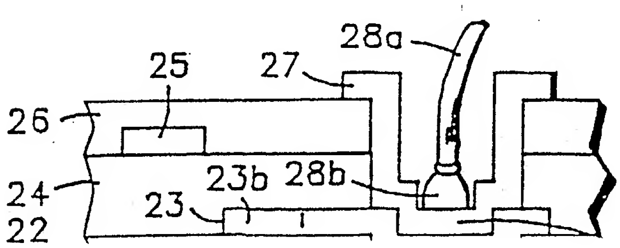

FIG. 2E

FIFTH MASK

– PRIOR ART –

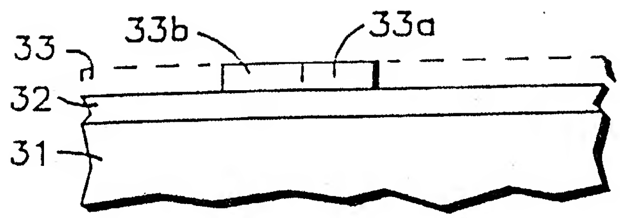

FIG. 3A

FIRST MASK

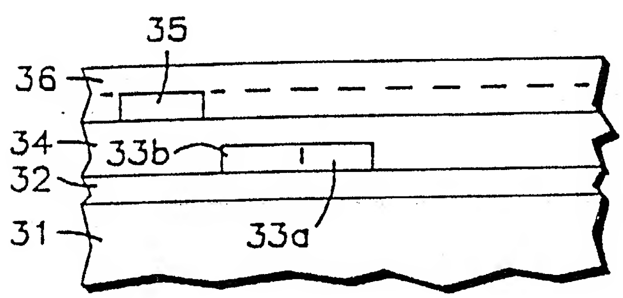

FIG. 3B

SECOND MASK

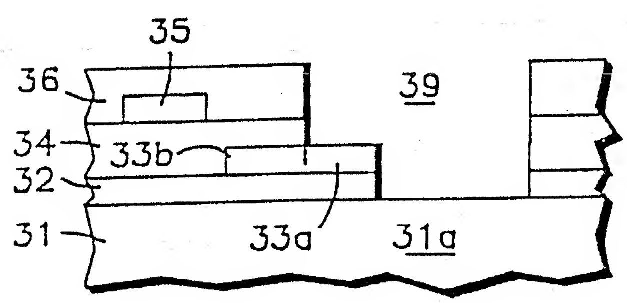

FIG. 3C

THIRD MASK

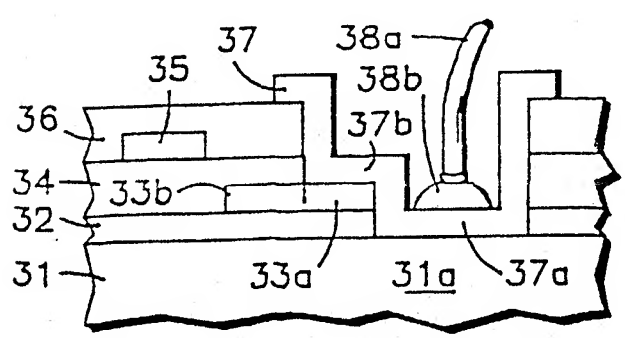

FIG. 3D

FOURTH MASK

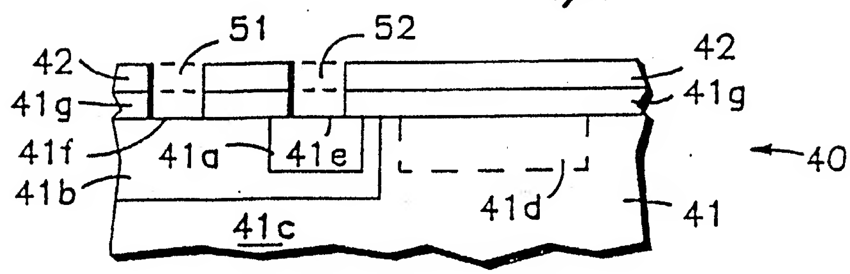

FIG. 4A

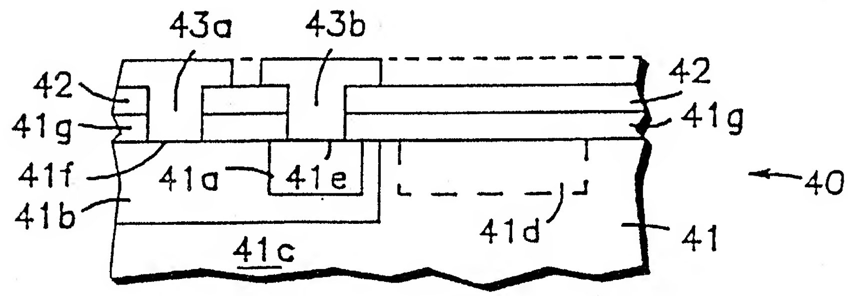

FIG. 4B

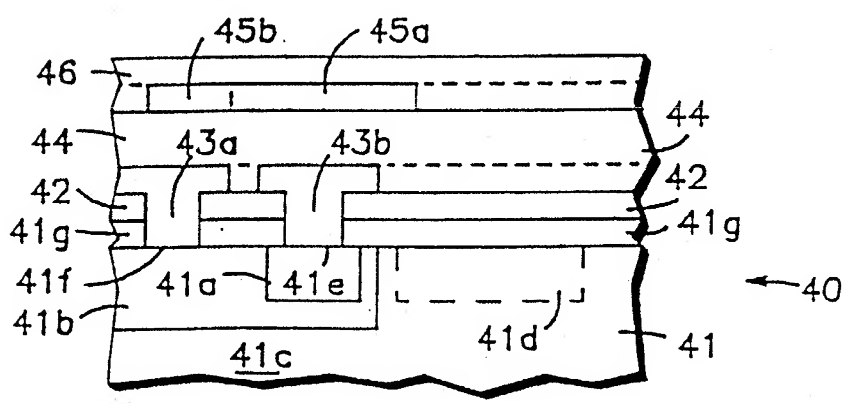

FIG. 4C

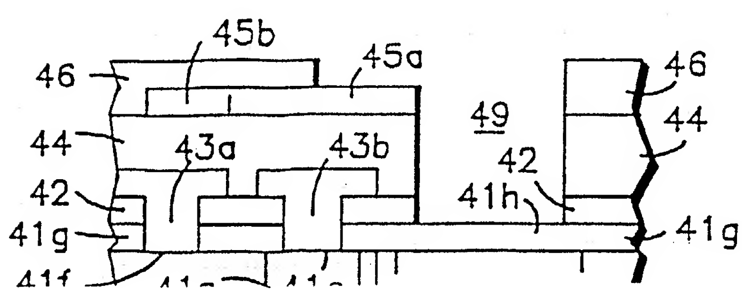

FIG. 4D

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/00472

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3] H 05 K 1/18, H 05 K 3/46
US 361/408 , 29/843

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	29/843, 846, 850 174/68.5; 361/403, 408, 414

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X,Y	US,A, 3,400,210 (Reimer) 03 September 1968	1 to 5,6 to10
X	US,A, 3,996,430 (Eberwein) 07 December 1976	1 to 5
A,Y	US,A, 3,955,023 (Blakely) 04 May 1976	1 to 5,6 to10
A,Y	US,A, 3,319,317 (Roche) 16 May 1967	1 to 5,6 to10
A,Y	US,A, 3,052,823 (Anderson) 04 September 1962	1 to 5,6 to10
Y	N, INTERNATIONAL BUSINESS MACHINES TECHNICAL DISCLOSURE BULLETIN, PUBLISHED MARCH 1982, (BEDETTI ET AL) EC PAD DESIGN USING POLYMIDS PACKAGE, VOLUME 24 NUMBER 10, PAGES 5113 and 5114.	

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
July 5, 1983	21 JUL 1983
International Searching Authority [1]	**Signature of Authorized Officer [10]**
ISA/US	Richard R [illegible]

International Application No. PCT/US83/00472

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ______, because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ______, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☒ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.